# Blog:

Joyce:

<https://digilent.com/reference/programmable-logic/nexys-2/start#:~:text=Nexys2%20circuit%20board%20is%20a,a%20Xilinx%20Spartan%203E%20FPGA>.

<https://digilent.com/reference/programmable-logic/nexys-3/start>

<https://digilent.com/reference/programmable-logic/nexys-4/start>

<https://digilent.com/reference/programmable-logic/nexys-a7/start>

Christal:

<https://link.springer.com/article/10.1007/s11265-017-1229-7>

Tyran:

<https://forum.digilent.com/topic/4972-audio-processing/>

<https://www.hackster.io/adam-taylor/audio-processing-with-the-snickerdoodle-727c40>

<https://www.analog.com/en/products/adau1761.html>#

Phalo:

(*ADAU1761 Datasheet and Product Info | Analog Devices*, n.d.; *Audio Processing - FPGA - Digilent Forum*, n.d.; *Audio Processing with the Snickerdoodle - Hackster.Io*, n.d.; *Nexys 2 - Digilent Reference*, n.d.; *Nexys 3 - Digilent Reference*, n.d.; *Nexys 4 - Digilent Reference*, n.d.; *Nexys A7 - Digilent Reference*, n.d.; Reiche et al., 2017)

*ADAU1761 Datasheet and Product Info | Analog Devices*. (n.d.). Retrieved April 29, 2022, from <https://www.analog.com/en/products/adau1761.html>#

*Audio processing - FPGA - Digilent Forum*. (n.d.). Retrieved April 29, 2022, from <https://forum.digilent.com/topic/4972-audio-processing/>

*Audio Processing with the Snickerdoodle - Hackster.io*. (n.d.). Retrieved April 29, 2022, from <https://www.hackster.io/adam-taylor/audio-processing-with-the-snickerdoodle-727c40>

*Nexys 2 - Digilent Reference*. (n.d.). Retrieved April 29, 2022, from <https://digilent.com/reference/programmable-logic/nexys-2/start#:~:text=Nexys2%20circuit%20board%20is%20a,a%20Xilinx%20Spartan%203E%20FPGA>

*Nexys 3 - Digilent Reference*. (n.d.). Retrieved April 29, 2022, from <https://digilent.com/reference/programmable-logic/nexys-3/start>

*Nexys 4 - Digilent Reference*. (n.d.). Retrieved April 29, 2022, from <https://digilent.com/reference/programmable-logic/nexys-4/start>

*Nexys A7 - Digilent Reference*. (n.d.). Retrieved April 29, 2022, from <https://digilent.com/reference/programmable-logic/nexys-a7/start>

Reiche, O., Özkan, M. A., Hannig, F., Teich, J., & Schmid, M. (2017). Loop Parallelization Techniques for FPGA Accelerator Synthesis. *Journal of Signal Processing Systems 2017 90:1*, *90*(1), 3–27. <https://doi.org/10.1007/S11265-017-1229-7>

# Milestone 2:

<https://www.nwengineeringllc.com/article/what-is-a-circuit-schematic.php>

<https://digilent.com/reference/programmable-logic/nexys-a7/start>